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Measurement and Analysis of GaAs MESFET Parasitic Capacitances

R. Anholt and S. Swirhun

Abstract—**From *S*-parameter measurements and subsequent equivalent-circuit parameter extraction for a series of 0.25 μm, ion-implanted GaAs MESFET's with different widths and different gate–source and drain–source spacings, parasitic FET pad capacitances and interelectrode capacitances have been separated from active-FET capacitances. The active-FET fringe capacitances extracted at pinch-off are compared with results from two-dimensional Poisson simulations.**

I. Introduction

It is well known that FET capacitances do not vanish at very negative gate voltages, and FET f_t values do not scale inversely with gate length for constant doping. One reason for these two observations is the presence of parasitic capacitance coming from three components: capacitance on the fringe of the gate in the semiconductor, interelectrode capacitance over the top of the semiconductor, and pad capacitance associated with the measurement. Any measurement technique, be it low-parasitic-on-wafer or bonded-FET *S*-parameter, requires the presence of pads for the probes or bond wires and interconnect metal to the active FET fingers. These elements add parasitic capacitance, which for small-gate-width, small-gate-length FET's can be comparable in magnitude to the active-FET capacitances. Extrapolating measured FET equivalent-circuit parameters (ECP's) for one width and layout to another assuming that the ECP's vary linearly with width in neglect of pad capacitances and inductances is a potential source of error.

Parasitic capacitances are most accurately measured in pinched FET's, where the FET capacitances that scale as the gate length are zero. Two models of the active-FET capacitances have been used. Wasserstrom and McKenna [1] found that the total active-FET fringe capacitance ($C_{gs}+C_{gd}$) is 0.177 pF/mm, independent of the doping, gate length, gate bias, and all other technological parameters. We have examined pinched-FET data from nine different foundries, and always find larger values, in part because of the components from the pad layout, which are not easy to compute. One motivation of the present work is to isolate the three components of parasitic capacitance so that just the active-FET capacitance modeled by Wasserstrom and McKenna can be compared.

The other model of parasitic GaAs FET capacitances is based on electrostatic solutions to Laplace's equation [2]–[5], often obtained in closed form in terms of elliptical integrals [4], [5]. These formulas predict that the interelectrode capacitances depend on the electrode spacing. Formulas such as this were recently applied to computing pinched-FET capacitances for microwave-switching devices [5] where the frequency figure of merit is inversely proportional to the pinched-FET capacitance. In this paper we show such formulas are indeed applicable for undoped GaAs MESFET's, but active-FET capacitances must be computed using techniques similar to those of Wasserstrom and McKenna. We show that even the interelectrode capacitance over the top of the semiconductor cannot be computed with electrostatic formulas; rather it is dominated by the capacitance in the semiconductor.

In this paper we derive a scalable FET model [6]; i.e., capacitances are modeled as $aW+b$, where W is the FET width and a and b are constants. Most circuit modeling programs allow ECP's to be modeled as a linear function of width (aW or $a'W^{-1}$ for resistances) and even allow W to be optimized. However, unless the intercept b is taken into account, varying the width can lead to substantial errors. In particular for our 0.25×100 μm^2 FET's, scaling the pinched-FET C_{gs} to 200 μm without accounting for the intercept leads to a 21% error. Also, it must be realized that the FET embedded in a circuit is coupled by microstrips with their own capacitances that the circuit simulators attempt to compute; hence the constant component that is present in the *S*-parameter measurement is different or absent in the circuit. Not all designs may be sensitive to this fact, but designers should be aware of the presence of the intercept capacitance in scaling FET designs.

II. Fabrication, Measurement, and Analysis Methods

The MESFET's characterized here were fabricated at the Honeywell Systems and Research Center with a conventional

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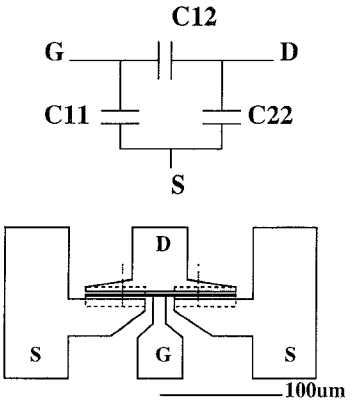

Fig. 1. FET layout and equivalent circuit for pinched FET's. The dashed line denotes the implanted region for 100-μm-width FET's. The dotted vertical line shows where the drain and gate metal and implanted regions are cut to produce 40-μm-width FET's (the source metal stays the same).

3-in., stepper-based, ion-implanted, recessed-gate fabrication technology designed for Ka-band, low-noise amplifier applications. The implant and processing were optimized for low-noise figures near 25% of I_{dss}. The present FET's had 90 and 40 keV dual Si implants and 80 keV Be buried p-layer implants, and were furnace annealed under Si_3N_4 caps. I_{dss} and g_m uniformity near 10% was achieved. All gate patterns were written in single-layer PMMA by electron-beam lithography and were recess etched; the gates were formed with a 0.4-μm-thick Ti/Pt/Au stack. FET passivation consisted of 0.2 μm Si_3N_4 deposited with plasma-enhanced CVD. Implant isolation was used.

The FET's were laid out in a standard T layout (Fig. 1) on unthinned (500 μm) wafers and were probed with 100-μm-pitch Cascade Microtech ground-signal-ground probes using an HP8510 network analyzer. The network analyzer calibration was performed using a Cascade Microtech–supplied impedance-standard substrate and the line-reflect-match method [7]. We measured FET's with gate widths of 40, 70, 100 μm (where the active layer and drain electrode widths also scaled), FET's with gate–source spacings of 0.54 to 1.6 μm (width = 100 μm, drain–source spacing = 2.5 μm), and FET's with drain–source spacings of 2 to 4 μm (width = 100 μm, gate–source spacing = 0.6 μm). For each FET geometry, we also fabricated a "dummy FET," which is an FET with the same layout but without the active region (no selective ion implant) adjacent to the active FET. The gate lengths and metal electrode separations were measured on wafer using a scanning electron microscope.

At pinch-off and at any bias for dummy FET's, R_{ds} is very large, and the FET y parameters can be modeled as [8]

$$Y_{11} = j\omega(C_{11} + C_{12}) \qquad Y_{21} = Y_{12} = -j\omega C_{12}$$
$$Y_{22} = j\omega(C_{22} + C_{12}) \tag{1}$$

where C_{11} connects port 1 to ground, C_{22} connects port 2 to ground, and C_{12} connects ports 1 and 2 (Fig. 1). To extract C_{ij}, measured S parameters from 1 to 26 GHz were converted to Y parameters, the imaginary parts were divided by ω, and the resulting capacitances were averaged over frequency. In all cases we found the capacitances to be independent of frequency, except for random fluctuations, of the order of 2% to 4%, ultimately attributed to S-parameter measurement precision. The pinched-FET capacitances were measured at $V_g = -5$ and -4 V, and the dummy FET values were measured at -5 and $+0.5$ V to verify that they are indeed independent of bias, as expected. All measurements were made at $V_{ds} = 0$. In contrast to FET's biased for $V_{ds} > 0$, where the equivalent circuit contains over 12 often nonunique ECP's, there are only three parameters for pinched FET's, which are obtained exactly at every frequency point. The access resistances and inductances (R_s, L_s, etc.) which give impedances of the order of a few ohms at 10 GHz, can be neglected for pinched FET's because the capacitive reactances for the pinched FET's are orders of magnitude larger (and $R_{ds} \sim \infty$ and $g_m = 0$) [8].

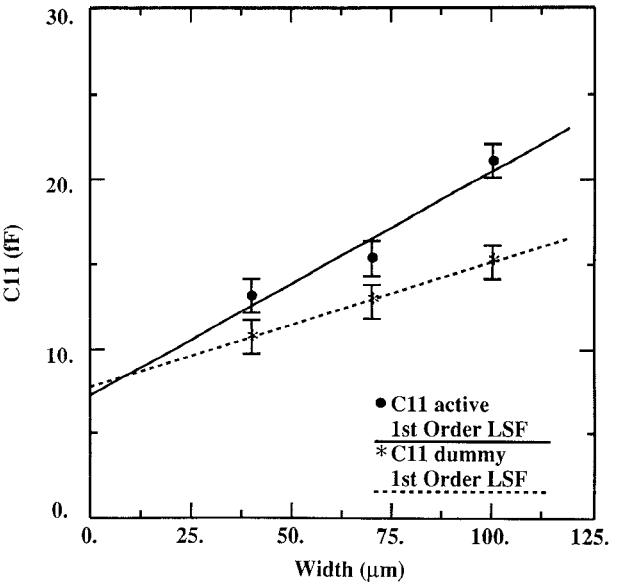

Fig. 2. C_{11} for FET's with widths of 40 to 100 μm and least-squares fits.

Only one set of FET's of each spacing and width was measured; hence we do not have sufficient statistical information to deduce the errors in the extracted capacitances. In other layouts, however, we measured over 100 pinched-FET capacitances per wafer and found typical variations of the order of 1 fF.

Each of the measured capacitances can be modeled using at least three components [6]:

$$C_{11} = C_{pg} + W(c_{gs1} + c_{gs2}) \qquad C_{12} = C_{pf} + W(c_{gd1} + c_{gd2})$$
$$C_{22} = C_{pd} + W(c_{ds1} + c_{ds2}) \tag{2}$$

where W is the FET width, c_{ij1} is interelectrode capacitance (per unit width) over the semiconductor surface, c_{ij2} is the component of capacitance through the semiconductor, and the C_p's, called pad capacitances, are assumed to be associated with **all** of the metal external to the active FET fingers. The difference between dummy FET's and active FET's should be in $c_{ij1} + c_{ij2}$; the pad capacitances should be the same, because away from the fingers, the dummy- and active-FET layouts are identical.

III. Results

Fig. 2 shows the active- and dummy-FET capacitances C_{11} for unpassivated FET's plotted against width. The intercepts of these curves are the pad capacitances, which are expected and within measurement errors are approximately the same for the active and dummy FET's. The slopes are given by the sum of

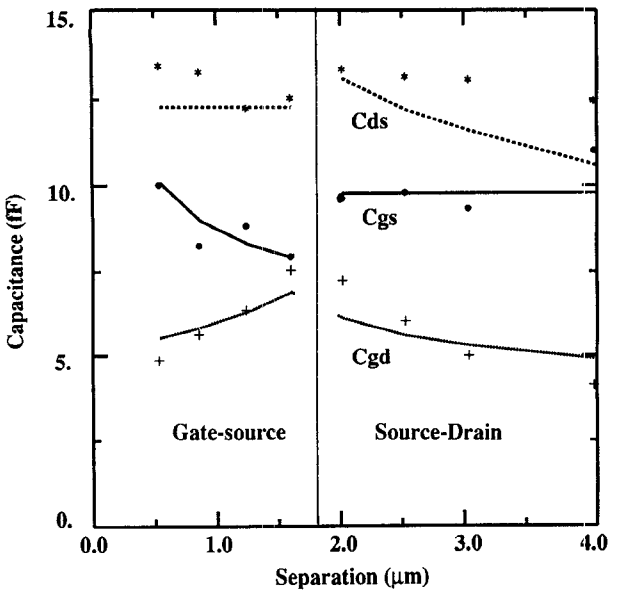

Fig. 3. Dummy-FET capacitances for 100 μm FET's versus gate–source or drain–source separations and modeled values based on eqs. (3) and (4). (The modeled values for C_{gd} were multiplied by 0.72.) The C_p's have been removed in the data.

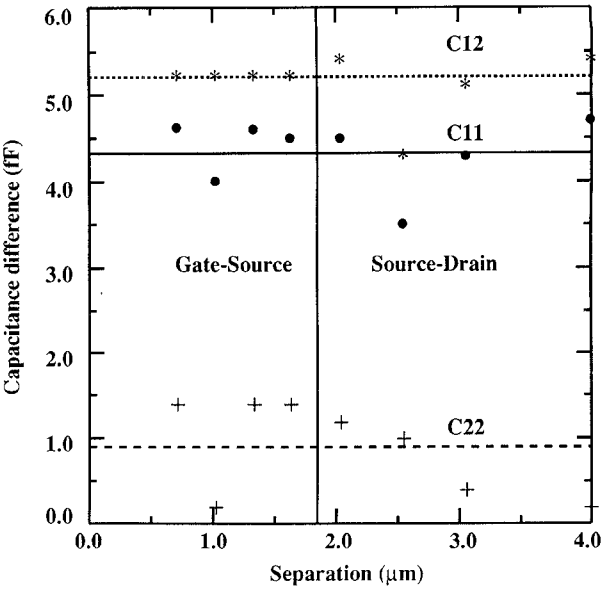

Fig. 4. Differences between passivated and unpassivated FET capacitances with the pad capacitances subtracted for 0.25×100 μm^2 FET's.

$c_{ij1}+c_{ij2}$ and are larger for the active FET's than for dummy FET's. For the unpassivated FET's, the resulting pad capacitances are taken as the average of the intercepts of the two curves: $C_{pg}=7.5$, $C_{pf}=2.5$, and $C_{pd}=2.8$ fF. For circuit modeling, the FET equivalent circuit is needed in isolation of the measurement pads and all other metal extrinsic to the FET fingers; therefore the active-FET capacitances should be reduced by these values.

The dummy-FET capacitances were measured for various gate–source and source–drain separations. The capacitances for $W=100$ μm FET's in Fig. 2 were obtained by subtracting the C_p values obtained above. For at least 15 years, some active FET capacitances (especially C_{ds} and C_{gd}) have been modeled using electrostatic formulas such as [4], [5]

$$C_{ij}=(\epsilon_r+1)\epsilon_0 WK\left(\sqrt{1-k^2}\right)\Big/K(k) \tag{3}$$

where

$$k_{ij}=\sqrt{\frac{L_{ij}}{L_{ij}+L_g}}, \qquad ij=gd \text{ or } gs$$

$$k_{sd}=\sqrt{\frac{(2L_s+L_{sd})L_{sd}}{(L_s+L_{sd})^2}}. \tag{4}$$

$K(x)$ is the elliptic integral, L_{ij} is the space between electrodes i and j, and L_s is the source electrode length. More complicated formulas have also been used [2], [3]. However, these formulas are only applicable to dummy-FET capacitances; they are not applicable to active-FET capacitances, which are governed by the Poisson equation instead of Laplace's equation. Fig. 3 shows that the dummy-FET C_{gs} and C_{ds} values are modeled reasonably accurately by these equations. For C_{gd}, however, it was necessary to multiply the model values by a factor of 0.72. The reason for this is not known.

The capacitances c_{ij1} and c_{ij2} can be separated by comparing pinched-FET capacitances (with the C_p's subtracted) before and after passivation. Passivation affects the interelectrode capacitance over the surface, but the pinched-FET capacitance in the semiconductor should be less affected. Fig. 4 shows the difference between the passivated and unpassivated active-FET capacitances versus the gate–source or drain–source spacings. When we began this work, we thought we could just use an electrostatic formula such as (3) to describe the interelectrode capacitance c_{ij1} over the top in both dummy and active FET's. This would give a difference that would depend on the spacing, as in Fig. 3. Clearly the differences in Fig. 4 are less dependent on spacing than the dummy-FET capacitances, indicating that the electrostatic formulas cannot be used to compute c_{ij1}.

At the semiconductor surface, the potentials must be continuous. Thus, one cannot use an electrostatic solution for the capacitance over the top of the semiconductor and a different Poisson-equation solution inside the semiconductor; the two solutions are coupled. The results in Fig. 4 suggest that the potentials in the semiconductor that give a spacing-independent capacitance dominate. The best way of describing c_{ij1} is to assume it is a factor $\epsilon_{\text{eff}}/\epsilon_r$ times c_{ij2}, where ϵ_r is the GaAs dielectric constant. For unpassivated FET's, the effective constant on top, ϵ_{eff}, is 1. For passivated ones, it should be less than or equal to the passivation dielectric constant, depending on passivation thickness [9]. For our 0.2 μm Si_3N_4 passivation ($\epsilon\sim7$), we find $\epsilon_{\text{eff}}=5.7$, 6.5, and 1.7 for C_{gs}, C_{gd}, and C_{ds}. The difference between C_{gs} and C_{gd} is mainly due to capacitance uncertainties of the order of 1 fF. This suggests that the field lines terminate over distances of the order of 0.2 μm for C_{gs} and C_{gd} but over larger distances for C_{ds}.

We can now isolate the active-FET capacitances c_{ij2} by subtracting the Cp's and multiplying the unpassivated values by $\epsilon_r/(\epsilon_r+1)$. Active-FET capacitances are expected to depend not on electrode–electrode distances but (for C_{gs} and C_{gd}) on the lateral extent of the electron depletion region from the gate edge. We also expect that $C_{gs}=C_{gd}$, and each should be one-half of the Wasserstrom–McKenna value, or 8.8 fF for 100 μm FET's [1]. As shown in Fig. 5, C_{gs} is on the average equal to C_{gd}, and no strong dependence on electrode distances is seen for C_{gs}, C_{gd}, or C_{ds}. The average value of C_{gs} and C_{gd} is 1.43

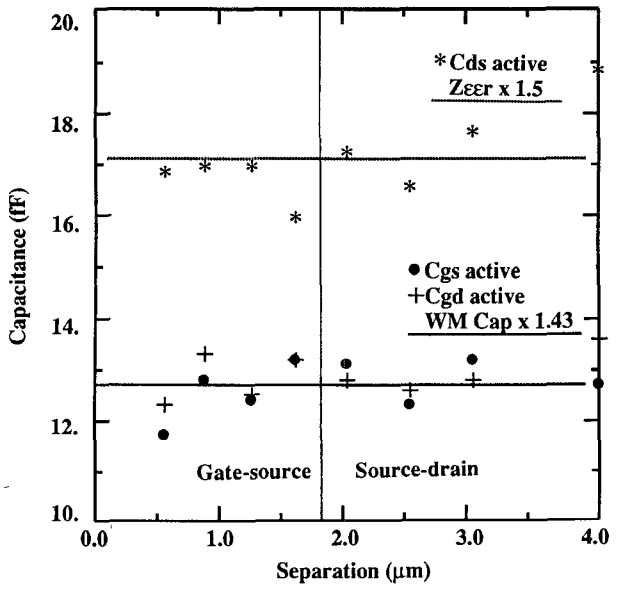

Fig. 5. Active-FET capacitances for 100 μm FET's versus gate–source or drain–source separations. The C_p's and c_{ij1} terms have been subtracted from the data.

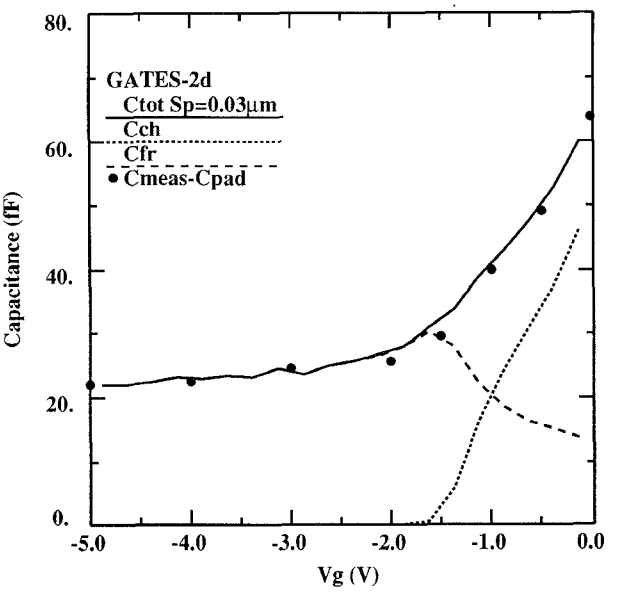

Fig. 6. Calculations of the sum of the active-FET C_{gs} and C_{gd} versus gate voltage. The two-dimensional Poisson solver GATES-2d computes the electron concentrations at all x, y coordinates, which were integrated. Then the capacitance was computed from the change in the total concentration divided by the change in gate voltage. The calculations assumed that the recess trench has 55° walls, is about 0.1 μm deep, and has a spacing of 0.03 μm between the edge of the gate and the trench. The data points have the C_p's and c_{ij1} terms removed.

times higher than the Wasserstrom–McKenna value, and C_{ds} is 1.5 times W($\epsilon_r + 1$) (0.18 pF/mm).

IV. Discussion

FET fringe capacitances in the semiconductor were modeled using a two-dimensional Poisson–Boltzman equation solver, GATES-2d [10], [11], which makes use of the GATES process model for GaAs MESFET technology. For uniformly doped flat FET's, GATES-2d predicts fringe capacitances that are identical to the Waserstrom–McKenna values. For recess etched FET's larger capacitances can be obtained if the space between the gate edge and the trench walls is very small. Then, below pinch-off, the gate potential can deplete electrons in the unrecessed region, and since there are more electrons there than in the etched region, higher fringe capacitances result. The exact gate-to-trench spacing is not known to better than ± 0.1 μm. Fig. 6 shows GATES-2d calculations of the sum of C_{gs} and C_{gd} in the semiconductor, where we have varied the gate–trench spacing until we fit the measured results. A 55° slope on the trench walls was assumed. The results indicate that the spacing must be about 0.03 μm on the average. We found that the computed sum capacitances decreased by 6 fF as the spacing changed from 0.01 to 0.1 μm.

Based on these results, we believe that the variations in the measured capacitances of the order of 1 fF probably stem from differences in the etching. Although reasonably uniform I_{dss} and threshold voltages were obtained for this wafer, small differences in the lateral etching can cause significant differences in the active-FET pinched capacitances.

Our extraction technique is similar to that of Dambrine *et al.* [8] and Mahon *et al.* [6]. Dambrine *et al.* assume that, for the pinched FET, $C_{pd} = C_{22}$, $C_{pf} = 0$ (thus $C_{12} = C_{gs2}$), and $C_{11} - C_{12} = C_{pg}$. For just modeling S parameters, it is immaterial how the component capacitances are separated, as long as the same total capacitance C_{11}, C_{12}, or C_{22} is obtained at every bias. The present technique is necessary to draw conclusions about the physical meaning of the capacitances. In particular, the Dambrine method leads to negative or near-zero active-FET C_{ds} values, as all of C_{ds} is assumed to be pad capacitance.

V. Conclusions

Much confusion is evident in the literature about the origin of FET parasitic capacitances and about ways to model these capacitances. This is the first work to show, by isolating the layout parasitics, where the electrostatic formulas are applicable and where the Poisson solutions are. The conclusion of this work is that in an active FET, the field lines both in the semiconductor and on top of the semiconductor terminate at the fringe of the gate, so that C_{gs} and C_{gd} are independent of the electrode separations. While the Poisson solution method of Wasserstrom and McKenna can be used to determine the fringe capacitance, the value is not constant, as they find, but depends on the gate bias and on the structure of the recess-etch trench.

We do not have a theory of C_{ds}. While previous ideas assumed it was all parasitic, the FET width dependence indicates that most of C_{ds} is associated with the active-FET fingers, and the spacing independence indicates that it is associated with the depletion region, instead of electrode spacings. Also the passivated–unpassivated difference gives a small effective passivation dielectric constant, implying that the relevant distances over which C_{ds} operates is larger than the passivation thickness, 0.2 μm.

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